Distributed Numerical Modeling of Dual-Gate GaAs MESFET's

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Abstract — A one-dimensional, numerical gradual channel model is used to examine the behavior of dual-gate GaAs metal–semiconductor field-effect transistors (MESFET's). Lumped circuit models for the dual-gate FET are based upon two single-gate devices with their channels in series and are considerably more complex than those for a single-gate device. By contrast, distributed numerical models for dual-gate devices do not incur any significant changes over equivalent single-gate device models. Such distributed numerical models are very useful for examining the regions of operation of each channel, the internal field distributions, and are also applicable to the case where the close proximity of the two gates couples the parameters of the individual channels and invalidates the modeling of the device as two channels in series.

NOMENCLATURE

F_{nx}	Electron flux through channel slice.
h	Gate depletion depth.
I_d	Drain current.
k	Transconductance parameter.
k_B	Boltzmann's constant.
L	Gate length.
m^*	Electron effective mass.
n	Electron density.
$\overline{N}$	Electron number per unit channel length (carrier cross section).
$\overline{N}_d$	Donor ion number per unit channel length.
$\overline{P}_x$	Electron momentum per unit channel length.
q	Electronic charge.
T	Absolute temperature.
T_e	Electron temperature.
$\overline{T}_e$	Average electron temperature over channel slice.
v_x	Electron velocity.
V_{DS}	Drain-to-source voltage.
V_{GS}	Gate-to-source voltage.
V_T	Threshold voltage.
Z	Gate width.
ϵ	Permittivity of semiconductor.
$\overline{\theta}$	Electron energy per unit channel length.
$\overline{\theta}_0$	Equilibrium electron energy per unit channel length.
τ_e	Electron energy relaxation time.
τ_m	Electron momentum relaxation time.
τ_{12}	Relaxation time for upward intervalley transfer.
τ_{21}	Relaxation time for downward intervalley transfer.
ϕ	Electrostatic potential at semiconductor surface.
ψ	Electrostatic potential in channel slice.

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I. INTRODUCTION

THE DUAL-GATE GaAs metal–semiconductor field-effect transistor (MESFET) has by virtue of its widespread usage been shown to be of great versatility and performance. Originally fabricated by Turner *et al.* [1], the device consists simply of two parallel, electrically independent gate electrodes crossing the channel region normally occupied by a single gate.

For use as a standard two-port, the dual-gate MESFET is normally connected in a common-source configuration with the input applied to the first gate, the second gate RF grounded, and the output taken from the drain. If a positive dc bias is applied to the second gate, then a significant improvement in the small-signal gain is obtained without a substantive loss in the unity-gain bandwidth [2]. This resulting small-signal gain is larger than that of a single-gate device of the same geometry and is a result of the dual-gate device effectively producing a two-stage cascode (common-source into common-gate) configuration. Additionally, the dual-gate MESFET exhibits a much improved decrease in the reverse feedback S_{12} parameter as a result of the electrostatic shielding that the second gate provides between the drain and the first gate. It has also been shown that the power gain and noise figure of the dual-gate MESFET can be simultaneously improved by making the second gate have a larger pinch-off voltage than that of the first [3]. Although this does improve the microwave performance, at least one additional processing step is required to achieve this, and consequently the majority of dual-gate devices have identical gates.

Current saturation in the dual-gate MESFET occurs when either of the two channels associated with the two gates individually saturates. As with a single-gate device, current saturation is produced through a combination of the geometrical constriction of the channel down to a minimum conducting cross section and the saturation of the electron velocity with field strength, with the latter dominating more for submicron gate lengths. When the channel of the first gate is saturated and the second is either saturated or unsaturated. the MESFET exhibits its

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highest transconductance. When the channel associated with first gate is not saturated, the overall device characteristics will still saturate with increased drain bias via the second channel, but with a significantly suppressed transconductance [4]. Through this mechanism, the conditions of the second channel can be used to control the small-signal parameters in the first channel.

With a variable dc bias applied to the second gate, a gain-controlled amplifier can be implemented [2], and with an RF signal applied to the second gate, the function of a mixer or modulator can be achieved [2], [5]. Indeed, one of the principal applications of the dual-gate MESFET has been a high-frequency mixer, which has typically achieved very high conversion gains even with low LO power, due to the strong nonlinearity of transconductance suppression by the second gate. By combining dual-gate MESFET's with 3 dB 90° hybrid couplers, high-efficiency image rejection mixers have been demonstrated [6]. Similarly, the mixing properties of the second gate have been used to construct frequency up-converters [7] and multipliers [8].

When the voltage at the second gate is sufficiently reduced, the associated channel will be pinched off and a high insertion loss will be introduced between the first gate and the drain. In this manner the second gate can be used as an RF switch on the output of the first channel. This has found usefulness in several novel applications that include microwave switches [9], phase shifters [10], and discriminators [11]. When the channel associated with the first gate is employed as the active element of an oscillator, the second gate can be used to mix in an RF signal [12] or multiply the output of the oscillator to give what has been termed an osciplier [13]. Because the input impedance of the first gate is largely unaffected by the bias conditions of the second gate while oscillating, the second gate can be used as a switch to selectively couple the oscillator's output to the drain terminal without the usual pulling of the oscillation frequency. This has been demonstrated in the construction of very low chirp pulsed RF oscillators, which are desirable for use in Doppler radar [14].

In addition to its analog microwave applications, the dual-gate GaAs MESFET is an important device in high-speed digital GaAs integrated circuits. When combined with a suitable load device between its drain and a positive supply rail, the dual-gate FET provides the basic logic function of a NAND gate within a very compact area. By contrast, the basic NOR function must be constructed by means of two paralleled inverter transistors working into the load device. While dual-gate FET's are central to digital logic NAND circuits of all families (NMOS, CMOS), they have been used in GaAs digital IC's principally with the early buffered FET logic (BFL) [15], [16] and with the more recent Schottky diode FET logic (SDFL) [17], [18]. As in the analog microwave case, the principal design limitation to using dual-gate MESFET's is understanding and predicting their operational regions, i.e., saturation versus nonsaturation of each of the two channels, so that the desired circuit behavior is obtained. For digital logic applications, this requires the current–voltage ($I-V$) characteristics to properly design the noise margins as well as the capacitance–voltage ($C-V$) characteristics of each gate to predict the nodal capacitances and switching speeds.

Lumped-element circuit models provide a straightforward and intuitive means of describing the gross large-signal behavior of both single- and dual-gate devices. Through the use of various "fitting parameters," they can be adjusted to accurately produce the $I-V$ characteristics and the more common small-signal parameters. Their usefulness, however, often fails when dynamic properties such as switching times, charge storage, and $C-V$ characteristics must be considered. Additionally, many second-order effects such as breakdown characteristics, subthreshold conduction, and interelectrode series resistances are poorly represented by lumped-element approaches. These usually require a distributed model of the FET channel that allows the various profiles of electric field, carrier concentration, and depletion depth to be calculated and visualized. While the distributed numerical modeling of single-gate JFET's and MESFET's has been the subject of an intensive effort of many researchers since the original two-dimensional analysis of Kennedy and O'Brien [19], [20], the dual-gate MESFET has so far been neglected in studies of this type.

This paper presents the first distributed numerical analysis of the dual-gate GaAs MESFET. Aside from the obvious need to specify the boundary value potential at a second gate electrode, the numerical modeling of a dual-gate FET incurs no additional complexities or computation time over equivalent simulations of single-gate devices. By contrast, lumped-element circuit models of the dual-gate FET are based upon the series connection of two single-gate FET's with the added disadvantage of the controlled current sources, and hence the small-signal parameters, being functions of conditions in both gated channels. This is particularly true for second-order corrections such as the interelectrode series resistance between the two gates (or channels), which depends strongly upon the depletion depths at each gate as well as the surface depletion of the channel layer between. Section II of this paper derives the simplified conditions for saturation and nonsaturation of each gated channel of the dual-gate FET based upon the series connection of two single-gate devices. This load-line approach has been found to be very useful for analyzing switching as well as RF bias conditions. Section III describes the model and method used in a numerical gradual channel analysis of the dual-gate FET. The results of this analysis method are presented in Section IV. Discussion and conclusions are presented in Section V.

II. Simplified Circuit Model and Load-Line Analysis

A first-order description of the dual-gate MESFET can be constructed through the series connection of the channels of two single-gate devices as indicated in Fig. 1. Such a model was first used by Liechti [2] and provides a simple basis for determining the operating point of each gated channel. As discussed previously, proper utilization of the

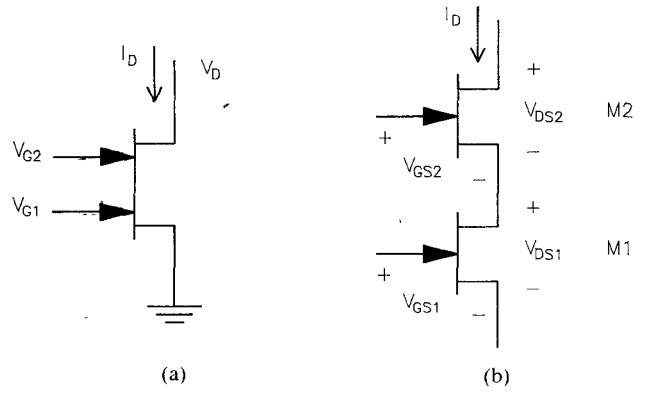

Fig. 1. (a) Circuit symbol for dual-gate MESFET. (b) Equivalent network composed of two single-gate MESFET's.

dual-gate FET relies upon both channels being biased into the correct operating region, and a good deal of insight into this can be provided by the simple circuit model of Fig. 1.

The simplest approximation is to describe the $I-V$ characteristics of the single-gate FET's, such as M1 in Fig. 1, by

$$I_{D,\text{nonsat}} = k\left(\frac{Z}{L}\right)\left[(V_{G1}-V_T)V_{DS1} - \frac{1}{2}V_{DS1}^2\right] \quad (1a)$$

$$I_{D,\text{sat}} = \frac{1}{2}k\left(\frac{Z}{L}\right)(V_{G1}-V_T)^2. \quad (1b)$$

By equating the terminal characteristics of the two circuit models of Fig. 1(a) and (b), $V_D = V_{DS1} + V_{DS2}$, $V_{G1} = V_{GS1}$, and $V_{G2} = V_{GS2} + V_{DS1}$. Thus, the $I-V$ characteristics of M2 become

$$I_{D,\text{nonsat}} = k\left(\frac{Z}{L}\right)\left[(V_{G2}-V_T-V_{DS1})(V_D-V_{DS1}) - \frac{1}{2}(V_D-V_{DS1})^2\right] \quad (2a)$$

$$I_{D,\text{sat}} = \frac{1}{2}k\left(\frac{Z}{L}\right)(V_{G2}-V_T-V_{DS1})^2. \quad (2b)$$

It is assumed that both M1 and M2 have identical threshold voltages and transconductance parameters. The second transistor, M2, will saturate for $V_D > V_{G2} - V_T$, which is notably independent of V_{DS1}. M2 will only be conducting for $V_{G2} - V_T > V_{DS1}$, but $V_D > V_{DS1}$ for any positive current flow I_D, so this condition is always satisfied. This feature conveniently allows the second transistor, M2, to be considered as a stationary load line for M1, as a function of the node voltage V_{DS1} between the two.

The $I-V$ characteristics of M1, and M2 which is regarded as the load line for M1, are plotted in Fig. 2. The saturated and unsaturated operational regions for both transistors give rise to four possibilities, all of which can be realized in a dual-gate FET. The operating point in each is determined by the intersection of the two FET $I-V$ curves. This figure shows that the largest channel currents are achieved for case (c), when M1 is unsaturated and M2 is

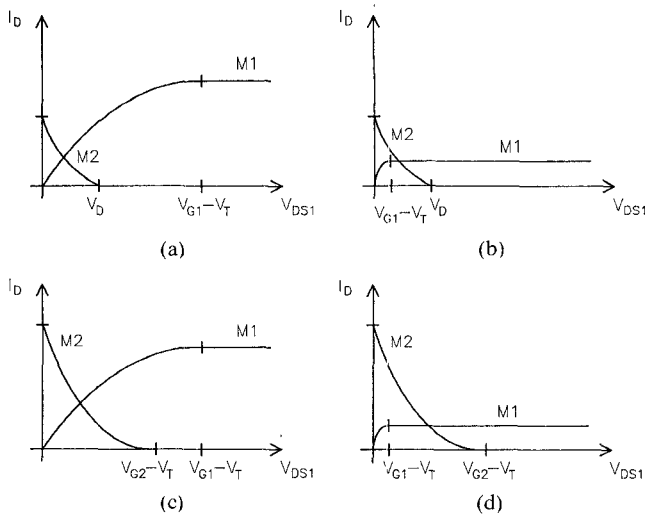

Fig. 2. Output characteristics of channel of first gate with load line created by channel of second gate. (a) M1 nonsaturated; M2 nonsaturated. (b) M1 saturated; M2 nonsaturated. (c) M1 nonsaturated; M2 saturated. (d) M1 saturated; M2 saturated.

saturated, but this also corresponds to the transconductance suppression region since the modulation of the channel by M1 is clamped by M2. It can also be observed from this representation that M1 saturates for $V_{G1} - V_T < (V_{G2} - V_T)/2$ if M2 is saturated and for $V_{G1} - V_T < V_D - V_D^2/2(V_{G2} - V_T)$ if M2 is not saturated.

The above load-line approach to determining the state of a dual-gate FET is useful for properly biasing the device and determining the signal swing at the internal node, as well as for determining the operational regions transited during a switching process. However, the above approach is also oversimplified by neglecting the finite output resistance in saturation and the parasitic series resistances associated with each electrode contact and the gate-to-gate interelectrode space. To address these effects, the model for each single-gate device can be augmented with parasitic circuit elements, but the resulting model for the dual-gate device no longer remains analytically tractable.

III. Numerical Gradual Channel Analysis

When second-order effects of the above-mentioned type must be included, the usual lumped-element circuit models lose much of their efficiency and insight and usually require the use of numerical circuit analysis programs to extract design parameters. Under these circumstances, where a more detailed and more accurate model is desired, particularly when the interest is in the internal electric fields and carrier fluxes, distributed numerical models must be used. These can be used to determine not only the terminal $I-V$ characteristics, but also the charge storage, carrier transit times, electric field distribution, and current densities which are needed to represent the transient and breakdown characteristics.

Numerical gradual channel models have in the past been used in the analysis of single-gate MESFET's and have allowed the use of full electron temperature and quasi-ballistic transport models [21]–[23]. These "quasi-two-dimen-

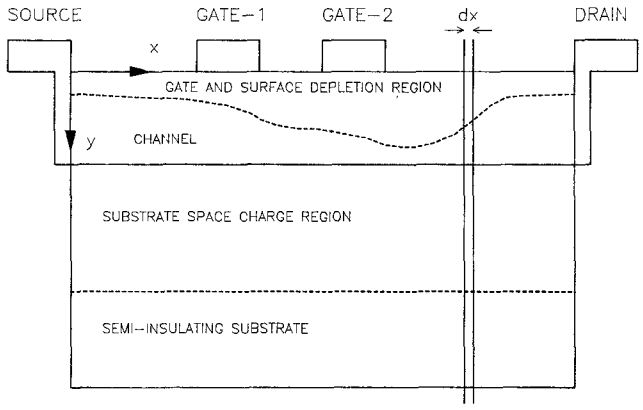

Fig. 3. Cross-sectional structure of dual-gate GaAs MESFET, coordinate system, and differential section of channel.

sional" models have generally been based upon the original gradual channel approximation of Shockley [24], which separates the problem into the transverse analysis of the gate depletion region followed by the longitudinal analysis of the channel itself, based upon the assumption that the electric field is orthogonally oriented in each of the two regions. Various two-dimensional effects have limited the applicability of this to short channel devices, but with suitable geometric corrections, it has been shown that such numerical models are fully rigorous and can be applied to the analysis of FET's even under the high electric field strengths normally associated with pinch-off and saturation of the channel [25].

The structure of a typical dual-gate MESFET is shown in Fig. 3. The device is assumed to be uniform in the z direction with an overall width of Z for both gates. To analyze this structure using a one-dimensional approach, the conducting channel is divided into differential slices of thickness dx, as shown in Fig. 3. With each differential slice, an electron density per unit channel length, termed the electron channel cross section, and an electron flux through the slice can be defined as

$$\bar{N}(x) = Z\int_0^\infty n(x, y)\, dy \tag{3}$$

$$F_{nx}(x) = Z\int_0^\infty v_x n(x, y)\, dy. \tag{4}$$

From these definitions, the channel current through the slice is

$$I = -qF_{nx} \tag{5}$$

the electron momentum associated with the flux is

$$\bar{P}_x = m^* F_{nx} \tag{6}$$

and the kinetic energy of the electrons per unit channel length is

$$\bar{\Theta} = \frac{1}{2}m^*\frac{F_{nx}^2}{N} + \frac{3}{2}\bar{N}k_B\bar{T}_e \tag{7}$$

where the average electron temperature is defined through

$$Z\int_0^\infty nk_B T_e\, dy = Zk_B\bar{T}_e\int_0^\infty n\, dy = \bar{N}k_B\bar{T}_e. \tag{8}$$

Balance equations for electron number, momentum, and energy density have been derived from the Boltzmann transport equation by Blötekjaer [26], [27]. By integrating these over the differential section dx of channel, analogous balance equations can be obtained for the electron number, momentum, and energy within the cross-sectional slice [25]. These are, respectively,

$$\frac{d}{dx}(v_x\bar{N}) = 0 \tag{9}$$

$$\frac{d}{dx}(v_x\bar{P}_x) = q\bar{N}\frac{d\psi}{dx} + \frac{d}{dx}(\bar{N}k_B\bar{T}_e) - \frac{\bar{P}_x}{\langle\tau_m(T_e)\rangle} \tag{10}$$

$$\frac{d}{dx}(v_x\bar{\Theta}) = qv_x\bar{N}\frac{d\psi}{dx} + \frac{d}{dx}(v_x\bar{N}k_B\bar{T}_e) - \frac{\bar{\Theta}-\bar{\Theta}_0}{\langle\tau_e(T_e)\rangle}. \tag{11}$$

These are supplemented by Poisson's equation, which takes the form

$$\frac{d^2\psi}{dx^2} = \frac{q}{\epsilon}(\bar{N} - \bar{N}_d) \tag{12a}$$

$$\bar{N}_d = Z\int_0^\infty N_d\, dy \tag{12b}$$

and the assumption has been made that the surface of each differential channel section is an equipotential. The case of general curvilinear equipotential surfaces has been discussed previously [25] and can be applied to this problem, but the solution is here phrased in rectangular coordinates for simplicity.

The above set of balance equations assumes conditions of dc steady-state operation, zero transverse injection of carrier number, momentum, or energy into the differential channel section, no generation or recombination of electrons, and no curvature of the field flux lines within the channel. For MESFET's of typical channel geometry, these effects do not overly restrict the model. Within this description, the above balance equations must be augmented with a channel gating function which specifies the available cross section of carriers as a function of the channel and electrode potentials. For otherwise unpassivated GaAs surfaces, the pinning of the Fermi level produces surface depletion which is normally encountered in most GaAs MESFET's. The effects of surface depletion on the channel gating function have been studied by Hariu [28], [29], who used a linearly interpolated surface potential between the electrodes to model the depletion regions on either side of the gate. Extending this model to the dual-gate MESFET gives the surface potential profile of Fig. 4. The surface potential is taken to be lower than the potential of the electrodes by an amount equal to the built-in voltage of the Schottky barrier. Between the electrodes the potential is linearly interpolated as shown. The difference between the surface potential profile and the channel potential profile sets the depletion depth h via

$$\psi - \phi = \frac{q}{\epsilon}\int_0^h N_d(y)\, y\, dy \tag{13a}$$

and the resulting cross section of electrons available for

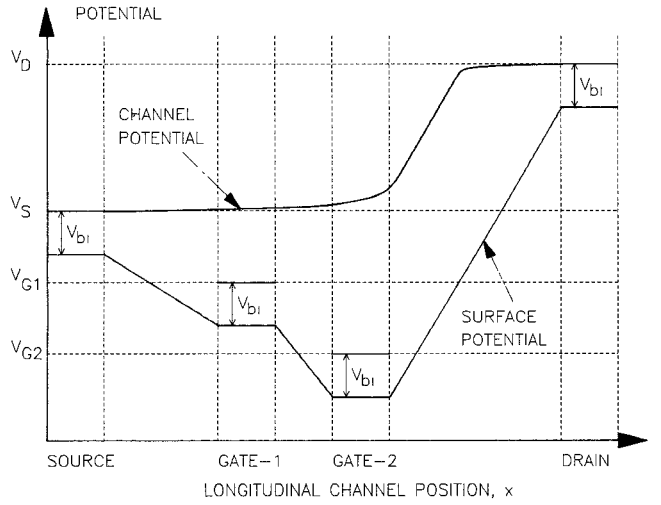

Fig. 4. Surface and channel potential profiles for the dual-gate MESFET, derived as an extension of Hariu's model [28], [29].

conduction in the differential channel section is then

$$\bar{N} = Z\int_h^\infty N_d(y)\,dy. \tag{13b}$$

The resulting system of equations, (9)–(13), gives a set of nonlinear ordinary differential equations in the variables of $\{\psi, v_x, \bar{N}, \bar{P}_x, \Theta\}$. These equations can be solved numerically by discretizing the domain of each variable, in this case x, and employing any of the many iterative techniques applicable to coupled nonlinear difference equations. In the present case, the domain was divided into 150 elements of equal size and the iterative solution was based upon a version of Gummel's algorithm [30]. This technique starts with an estimate of the channel potential profile and successively adds corrections to it so as to continually minimize a mean-squared error between successive potential profiles. Boundary values on the potential at the drain and the source are maintained by solving a one-dimensional Poisson equation, whose charge density is set by the predictor derivatives of the system of equations. Poisson's equation is then solved through the standard inversion of a tridiagonal matrix. This algorithm was implemented in Turbo-Pascal on an IBM PC-AT. The iterative solution of the electrostatic potential converged to within 0.01 kT/q after usually 10–12 iterations for typical bias values and took less than 15 seconds on an 8 MHz PC-AT.

IV. Application of Numerical Model

The gradual channel transport model of (9)–(13) was applied to a typical dual-gate GaAs MESFET structure consisting of two 0.5-μm-long gates separated by 0.5 μm with a source to gate-1 spacing of 1.0 μm and a drain to gate-2 spacing of 1.5 μm, as indicated in Fig. 3. The device was presumed to be epitaxially fabricated with an active channel layer uniformly doped to 5.0×10^{17} cm^{-3} and 0.1 μm thick. The mean electron momentum and energy relaxation times in (10) and (11) were taken to be explicit functions of the electron temperature and represent the combined effects of all the applicable scattering mechanisms in the zone-center (Γ) valley as well as intervalley electron transfer to the upper satellite (L) valleys. This gives an overshooting velocity versus field characteristic which has been used by previous authors to simulate electron transfer effects in other GaAs devices [23], [31]–[33] and which is described in the Appendix.

The results of the numerical model are shown in Figs. 5–16. Two cases have been considered: $V_{G1} > V_{G2}$ and $V_{G1} < V_{G2}$. As the drain voltage V_D is increased, the two cases cause the current to saturate due to current saturation individually from gate 2 and gate 1, respectively. For each case the channel profiles of potential, electric field, channel charge density, electron velocity, channel electron cross section, and electron temperature are plotted. Within these exist all four of the possible bias conditions described in Section II.

For the first case, where $V_{G1} > V_{G2}$, low values of drain bias place both channels, referred to as M1 and M2, into nonsaturation. The subsequent increase in V_D saturates only M2 because the resulting current flow through M1 is insufficient to cause a voltage drop through the channel of M1 that would induce pinch-off. This case behaves similarly to a single-gate MESFET with only a gate of M2, but with the channel resistance of M1 in series with its source. This corresponds to the common bias conditions for transconductance suppression, where the saturated current in M2 is effectively controlled by the voltage at the node between M1 and M2 (source of M2), which is itself set to the product of the channel current and channel resistance of M1. This configuration is equivalent to the small-signal modulation of the source bias resistor in the self-source-bias of a depletion-mode FET. Figs. 5–10 demonstrate that this series resistance, which loads and effectively modulates the source of a saturated M2, cannot be considered as only the resistance of the channel lying under the gate of M1, but rather must include the complete current path from the source electrode to the source side of the gate of M2. While this demonstrates the need for the inclusion of the interelectrode series resistances in a lumped-element model, the numerical results also indicate that these resistances are generally nonlinear, being a strong function of the conditions in both gated channels.

For the second case, where $V_{G1} < V_{G2}$, low drain bias voltages again place both M1 and M2 into nonsaturation. As the drain bias V_D is increased, M1 saturates first by presenting the largest constriction to the channel. As M1 saturates, the channel potential at the drain side of M1 reaches a maximum voltage, and further increases in V_D must be taken up across M2. This eventually saturates M2, with the channel potential existing between M1 and M2 adjusting itself to allow both gated channels to saturate. It is interesting that this is the one situation that produces two high-field regions within the channel and also two channel charge dipoles, as shown in Figs. 12 and 13.

The expansion of the high-field domain from underneath the gate and toward the drain with increasing drain bias is readily observable from the numerical results. It is

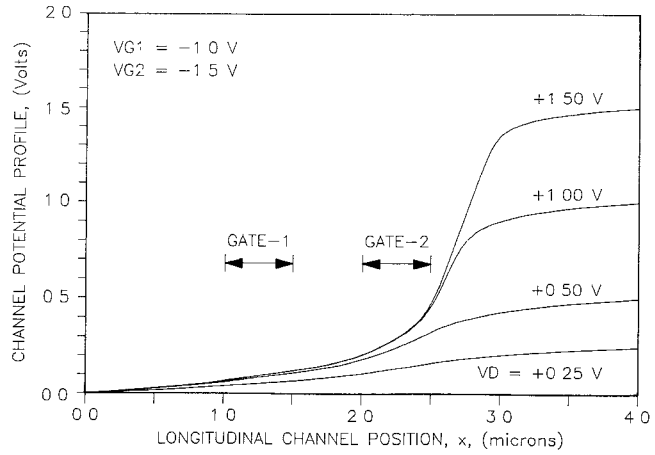

Fig. 5. Channel potential profiles for a 0.5×50 μm dual-gate GaAs MESFET on a 0.1-μm-thick active layer uniformly doped to 5×10^{17} cm^{-3} for the case of $V_{G1} > V_{G2}$.

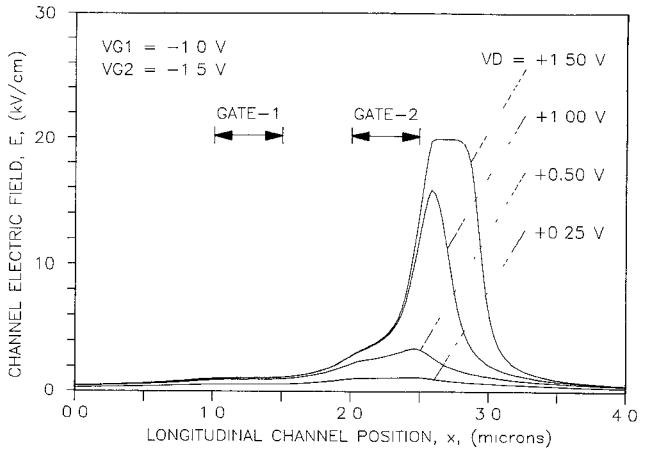

Fig. 6. Channel electric field profiles corresponding to those of Fig 5.

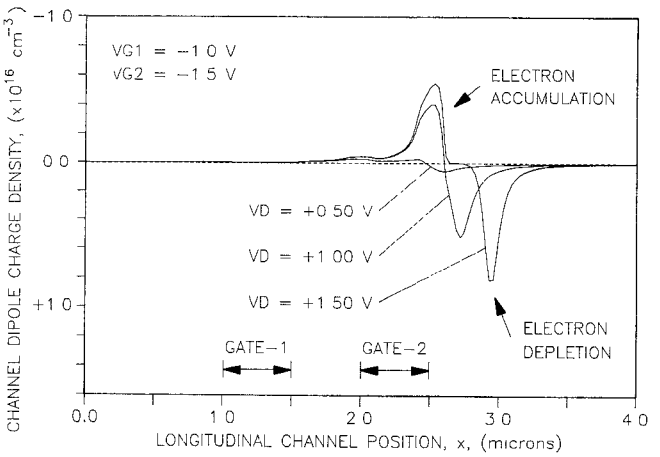

Fig. 7. Channel dipole charge density profiles corresponding to those of Fig. 5.

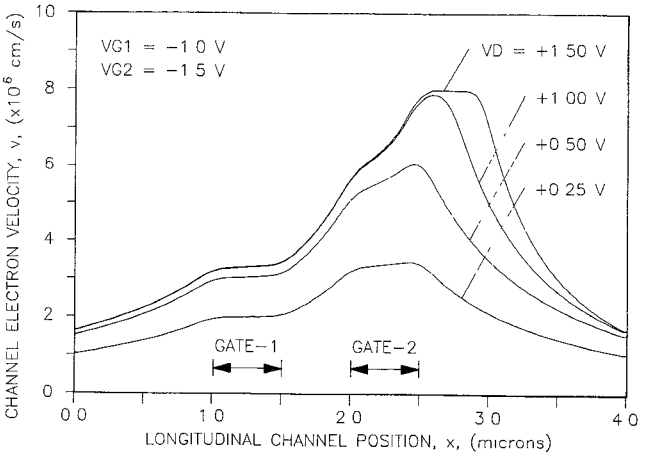

Fig 8. Channel electron velocity profiles corresponding to those of Fig. 5.

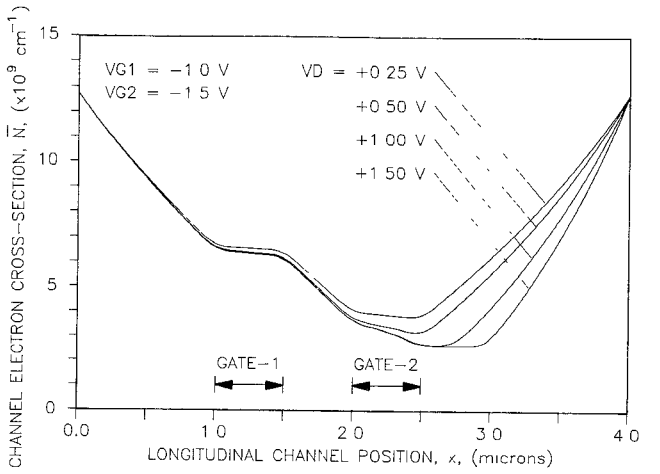

Fig 9. Channel electron cross-section profiles corresponding to those of Fig. 5

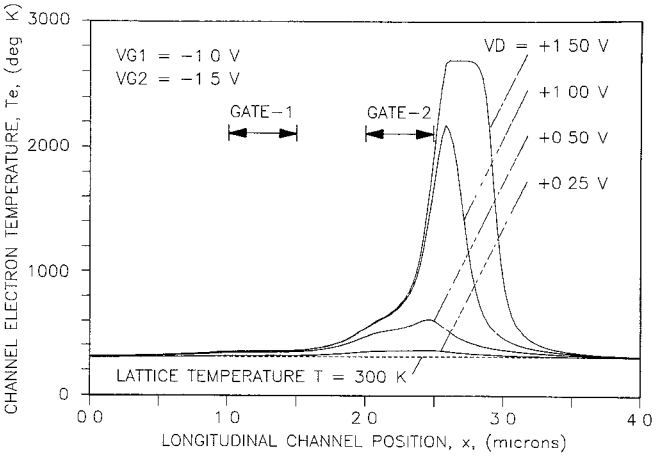

Fig. 10 Channel electron temperature profiles corresponding to those of Fig 5

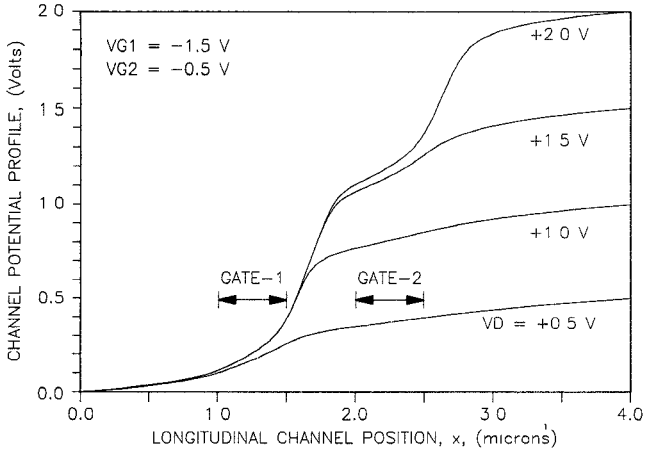

Fig. 11. Channel potential profiles for a 0.5×50 μm dual-gate GaAs MESFET on a 0.1-μm-thick active layer uniformly doped to 5×10^{17} cm^{-3} for the case of $V_{G1} < V_{G2}$.

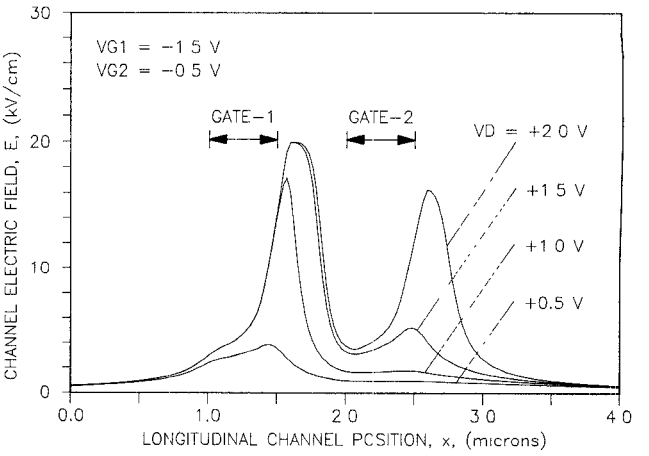

Fig. 12. Channel electric field profiles corresponding to those of Fig. 11.

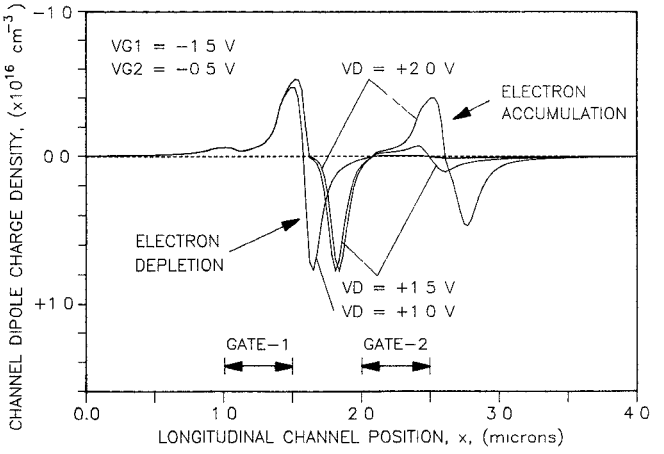

Fig. 13. Channel dipole charge density profiles corresponding to those of Fig. 11.

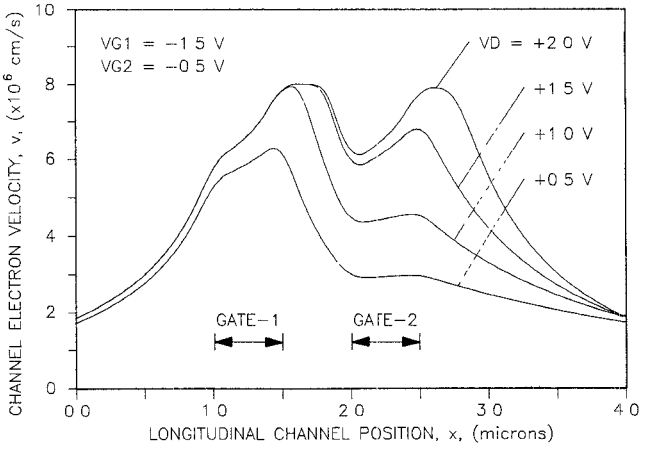

Fig. 14. Channel electron velocity profiles corresponding to those of Fig. 11.

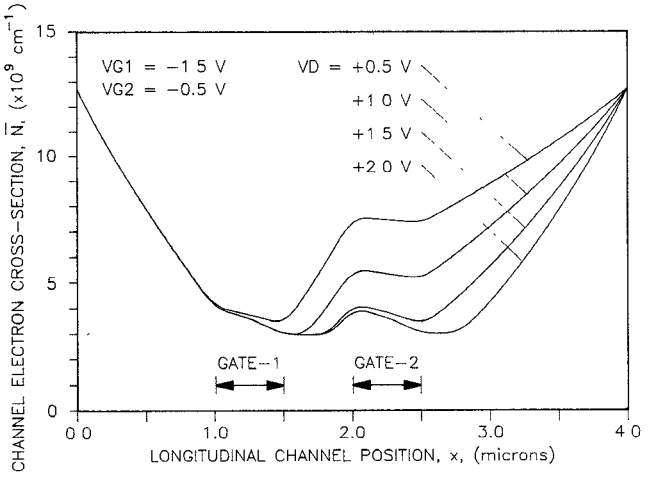

Fig. 15. Channel electron cross-section profiles corresponding to those of Fig. 11.

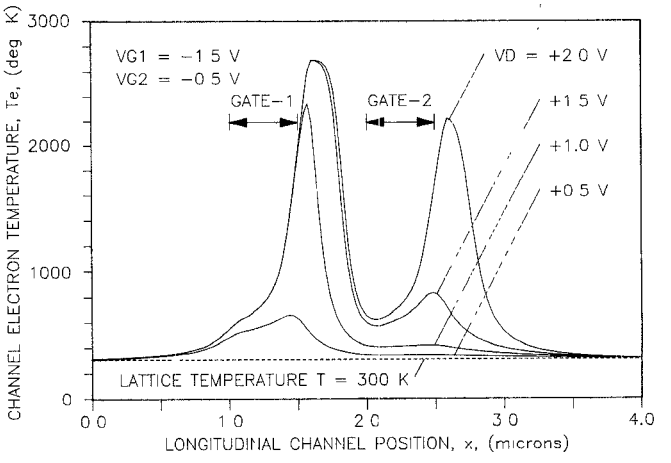

Fig. 16. Channel electron temperature profiles corresponding to those of Fig. 11

conceivable that if the two gates of a dual-gate FET were sufficiently close together then the high-field regions would fill the interelectrode space between the gates, effectively eliminating the associated series resistance. The numerical simulations help resolve this question. Fig. 12 shows that as V_D is increased, two very distinct high-field regions form successively at the drain edges of each gate and these two regions do not tend to merge together. While the minimum in the electric field between the gates is higher than its value near either the source or the drain, it still is only on the order of 5 kV/cm, placing the carrier transport into the warm electron range for GaAs. Fig. 14, however, indicates that the carrier velocity does not remain proportional to the channel field profile, as a result of both the nonohmic transport at warm electron temperatures and also the inertia maintained by the electrons transiting the region between the two high-field peaks. This latter contribution would be expected to be of more influence as the gate-to-gate spacing decreases. From these results it is apparent that the interelectrode spaces exert a considerable influence over the internal field distributions, but that they cannot be simply modeled as either a lumped-element series resistance or an extension of the gated region of either channel.

V. Discussion and Conclusions

The conduction properties of the interelectrode spaces modify the characteristics of single- and dual-gate FET's in a variety of ways. From the standpoint of lumped-element models, they have the effect of introducing series resistances to each electrode, and in the case of a dual-gate FET, between the two gated channels. For a single-gate FET, these series resistances increase the drain potential required for current saturation and decrease the value of gate potential required for channel pinch-off. For dual-gate FET's they additionally increase the effective source voltage at the second channel in the transconductance suppression region and increase the drain bias required to saturate both channels when $V_{G1} < V_{G2}$. For large-signal applications this ultimately limits the signal swing within the saturated current region. For small-signal applications, it is well known that series resistances degrade both the maximum available gain and the noise figure.

Distributed numerical models offer the advantage of being able to include the effects of the interelectrode spaces directly. In general, the inclusion of the drain-to-gate and source-to-gate interelectrode spaces as well as the second gate and gate-to-gate interelectrode space of a dual-gate device incurs no additional computational complexity over that of distributed numerical models of the gated part of a single channel alone. The inclusion of the same effects within a lumped-element circuit model greatly complicates both the large- and small-signal models and frequently requires a numerical approach to solve the resulting circuit. Hence, if a numerical approach is ultimately needed even for lumped-element models, then distributed modeling of the overall device can be quite competitive.

Additionally, the distributed numerical modeling of FET's is often necessary for accurate representation of the internal dynamic variables. For the present case of the dual-gate GaAs MESFET, it has been shown that the interelectrode region between the two gates cannot be treated as either a simple linear series resistance or an extension of the gated portion of either channel. The combined effects of surface depletion, current saturation nonlinearities, and hot electron transport require that these regions be described by means of a distributed approach, similar to the gated part of the channel. Future work in this area will be directed toward making these distributed models more convenient for circuit analysis and design.

Appendix
Relaxation Time Constant Model for GaAs

Figs. 17 and 18 give the momentum and energy relaxation time constants for electrons occupying the single Brillouin zone-center conduction band minima (Γ valley) of GaAs. The contributing scattering mechanisms include acoustic phonons, piezoelectrically coupled phonons, polar optical phonons, ionized impurities, and intervalley scattering to the upper satellite valleys lying at the L-symmetry points. The scattering rates for all of these processes can be obtained from the standard literature [34], [35], and they are taken here to be explicit functions of the electron temperature as shown. The energy band structure parameters, deformation potentials, and coupling constants used to evaluate these rates are the same as those that have been used for Monte Carlo simulation of electron transport in GaAs [36]. Other key material properties have been obtained from the review paper by Blakemore [37].

For the case of a uniform material with a uniform applied dc electric field, the balance equations (9)–(11) can be used to construct the velocity-field characteristic that is embedded within the momentum and energy relaxation time constants. Given an applied field strength, the resulting electron velocity and electron temperature can thus be determined from a simultaneous solution to

$$v_x = \frac{q\tau_m(T_e)}{m^*}\frac{d\psi}{dx} \tag{A1}$$

$$v_x q\frac{d\psi}{dx} = \frac{3k_B(T_e - T)}{2\tau_e(T_e)} \tag{A2}$$

which equates the rate of momentum transfer and carrier heating by the field to momentum loss and carrier cooling via scattering.

This yields a velocity saturating characteristic for electrons that are confined to the Γ valley. To include the effects of intervalley transfer, the intervalley scattering rates of Fig. 19 must also be included. If the density of carriers in the lower Γ valley is n_1 and in the upper satellite L valleys is n_2, then under steady-state conditions the upward and downward transition rates must be equal:

$$\frac{n_1}{\tau_{12}} = \frac{n_2}{\tau_{21}}. \tag{A3}$$

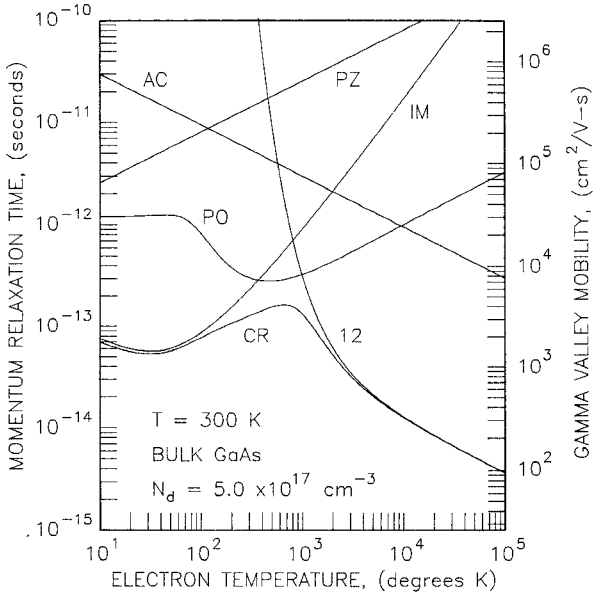

Fig. 17. Momentum relaxation time for the Γ valley of GaAs. Contributions to the combined rate (CR) are from acoustic phonons (AC), piezoelectrically coupled phonons (PZ), polar optical phonons (PO), ionized impurities (IM), and intervalley scattering (12).

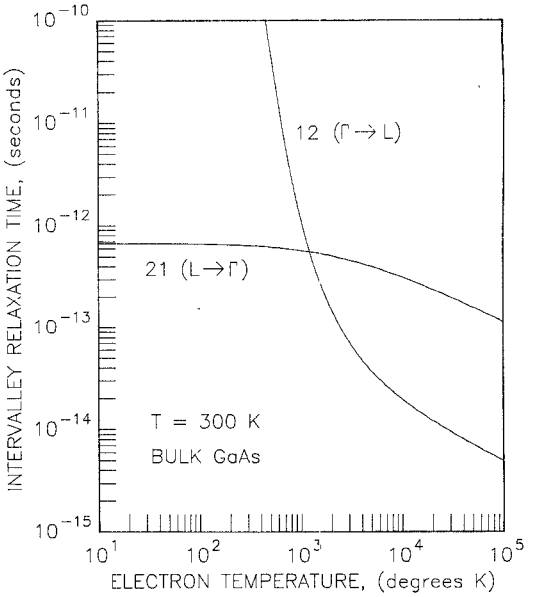

Fig. 19. Intervalley scattering relaxation times for GaAs. Under steady-state conditions, the ratio of the upward rate (12) to the downward rate (21) establishes the population fraction of electrons in each valley.

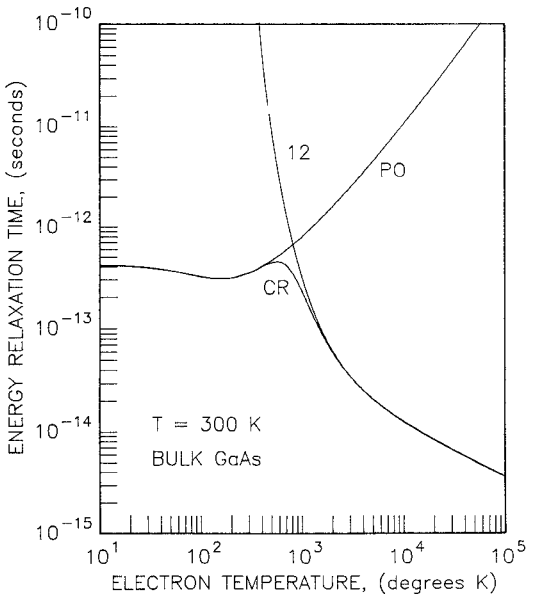

Fig. 18. Energy relaxation time for the Γ valley of GaAs. Contributions to the combined rate (CR) are from polar optical phonons (PO) and intervalley scattering (12).

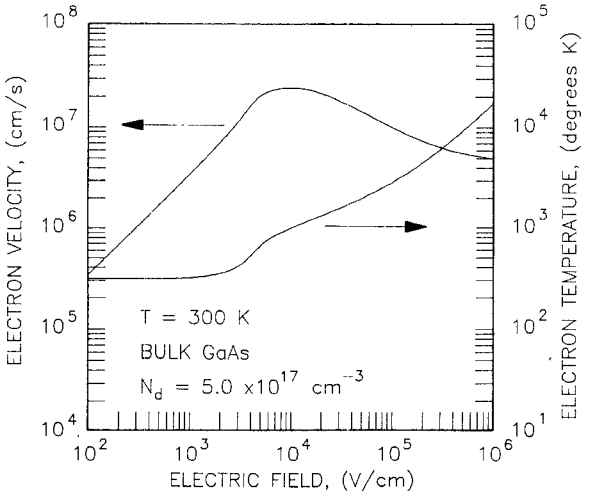

Fig. 20. Electron velocity and electron temperature versus applied electric field for GaAs. Curves correspond to the doped channel layer of the MESFET

Thus, the ratio of the intervalley scattering lifetimes as a function of electron temperature determines the fraction of the electron population occupying each valley for steady-state conditions. The momentum relaxation lifetime used in this work is the lifetime of Fig. 17 multiplied by the population fraction of carriers that reside within the Γ valley:

$$\tau_m = \frac{\tau_m^{\Gamma}}{1+\dfrac{\tau_{21}}{\tau_{12}}}. \qquad \text{(A4)}$$

The resulting velocity-field characteristic is shown in Fig. 20 and displays a peak overshoot velocity of 2×10^7 cm/s, which agrees with commonly accepted values [36], [37]. The peak occurs at a slightly higher than usual applied field of 8 kV/cm, due to the lower mobility caused by the high doping level of the channel layer.

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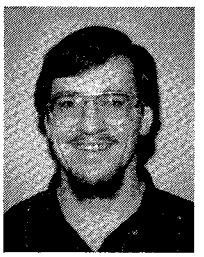

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